CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. An analog front end system, comprising:

a digital-to-analog converter;

a line driver, electrically coupled to said digital-to-analog converter;

a hybrid, electrically coupled to said line driver;

a multiple-input device having a plurality of inputs and at least one output, wherein at least one of said inputs is electrically coupled to said hybrid;

an analog-to-digital converter, electrically coupled to said output of said multiple-input device;

an isolation circuit configured to maintain direct-current isolation between the terminals of said isolation circuit, wherein:

said isolation circuit is electrically coupled to at least one of said inputs of said multiple-input device; and

said isolation circuit comprises a plurality of resistance elements and a plurality of capacitance elements, electrically coupled;

a ground circuit configured to provide a ground reference, wherein:

said ground circuit is electrically coupled to at least one of said inputs of said multiple-input device; and

said ground circuit comprises a plurality of resistance elements and at least one ground reference point, electrically coupled; and

a processing circuitry, said processing circuitry being configured to control said digital-to-analog converter, said line driver, said analog-to-digital converter, and said multiple-input device in response to commands received by said processing circuitry.

2. The analog front end system of claim 1, wherein said multiple-input device is configured such that said inputs are selectively operational.

3. The analog front end system of claim 1, wherein said multiple-input device is a multiplexer.

4. An analog front end system, comprising:

a digital-to-analog converter;

a line driver, electrically coupled to said digital-to-analog converter;

means for multiplexing a plurality of inputs to at least one output, electrically coupled to said line driver; and

an analog-to-digital converter, electrically coupled to said means for multiplexing.

5. The analog front end system of claim 4, further comprising a hybrid, electrically coupled between said line driver and one of said inputs of said means for multiplexing.

6. The analog front end system of claim 4, further comprising means for direct current isolation of said multiple-input device from an input terminal, electrically coupled to one of said inputs of said means for multiplexing.

7. The analog front end system of claim 4, further comprising means for providing a ground reference, electrically coupled to one of said inputs of said means for multiplexing.

8. The analog front end system of claim 4, further comprising means for controlling said digital-to-analog converter, said line driver, said analog-to-digital converter, and said multiple-input device responsive to commands received by said means for controlling.

9. An analog front end system, comprising:

a digital-to-analog converter;

a line driver, electrically coupled to said digital-to-analog converter;

a multiple-input device having a plurality of inputs and at least one output, electrically coupled to said line driver; and

an analog-to-digital converter, electrically coupled to said multiple-input device.

10. The analog front end system of claim 9, further comprising a hybrid, electrically coupled between said line driver and said multiple-input device.

11. The analog front end system of claim 9, further comprising an isolation circuit, electrically coupled to said multiple-input device.

12. The analog front end system of claim 11, wherein said isolation circuit comprises a plurality of resistance elements and a plurality of capacitance elements, electrically coupled.

13. The analog front end system of claim 9, further comprising a ground circuit configured to provide a ground reference, electrically coupled to said multiple-input device.

14. The analog front end system of claim 13, wherein said ground circuit comprises a plurality of resistance elements and at least one ground reference point, electrically coupled.

15. The analog front end of claim 9, wherein said multiple-input device is configured such that said inputs are selectively operational.

16. The analog front end system of claim 9, further comprising a processing circuitry, said processing circuitry being configured to control said digital-to-analog converter, said line driver, said analog-to-digital converter, and said multiple-input device in response to commands received by said processing circuitry.

17. A method for testing a DSL line, comprising the steps of:

transmitting test samples to an analog front end;

interpreting said test samples as multi-bit digitized values using said analog front end;

generating test patterns, from said digitized values, having a plurality of samples; and

testing a DSL line using said test patterns.

18. The method of claim 17, wherein said interpreting step comprises interpreting said test samples as 8-bit digitized values using said analog front end.

19. The method of claim 17, wherein said interpreting step, said generating step, and said testing step are controlled by a processing circuitry responsive to received commands.

20. A method for DSL line testing, comprising the steps of:

providing test stimuli to a DSL line using an analog front end; and

receiving responses to said test stimuli from said DSL line using said analog front end.

21. The method of claim 20, wherein said providing step comprises providing test stimuli to a DSL line using a digital-to-analog converter and an analog-to-digital converter of said analog front end.

22. The method of claim 20, wherein said providing step comprises transmitting test stimuli to a DSL line on a carrier signal using an analog front end.

23. The method of claim 20, wherein said receiving step further comprises storing said responses to said test stimuli to a computer.

24. A DSL line testing format, comprising:

a plurality of test frames, wherein:

said test frames comprise a plurality of multi-bit test samples; and

the first of said samples of said test frames comprises a test header.

25. The testing format of claim 24, wherein said test header comprises a test control header format.

26. The testing format of claim 24, wherein said test header comprises a test status header format.

27. A test header, comprising:

a multi-bit test control header format, said test control header format comprising:

a pattern length field configured to control the generation of a plurality of test patterns by an analog front end;

a sample rate field configured to control the selection of sample rates of a digital-to-analog converter and of an analog-to-digital converter;

a spare field, capable of being configured to control at least one function of an analog front end;

a loop-back field configured to control a loop-back function of an analog front end;

a hybrid field configured to control the operating status of a hybrid of an analog front end; and

an input select field configured to control the selection of a plurality of test inputs to an analog front end.

28. The test header of claim 27, wherein said test control header format is 12-bits long.

29. The test header of claim 28, wherein:

said pattern length field is 4-bits long;

said sample rate field is 2-bits long;

said spare field is 2-bits long;

said loop-back field is 1-bit long;

said hybrid field is 1-bit long; and

said input select field is 2-bits long.

30. The test header of claim 27, further comprising a buffer configured to store test samples.

31. A test header, comprising:

a multi-bit test status header format, said test status header format comprising:

a pattern length field configured to provide identification of one or more of a plurality of test patterns generated by an analog front end;

a sample rate field configured to provide the selection status of sample rates of a digital-to-analog converter and of an analog-to-digital converter;

a spare field, capable of being configured to provide the status of at least one function of an analog front end;

a loop-back field configured to provide the status of a loop-back function of an analog front end;

a hybrid field configured to provide the operating status of a hybrid of an analog front end; and

an input select field configured to provide the selection status of a plurality of test inputs to an analog front end.

32. The test header of claim 31, wherein said test status header format is 12-bits long.

33. The test header of claim 32, wherein:

said pattern length field is 4-bits long;

said sample rate field is 2-bits long;

said spare field is 2-bits long;

said loop-back field is 1-bit long;

said hybrid field is 1-bit long; and

said input select field is 2-bits long.

34. The test header of claim 31, further comprising a buffer configured to store test samples.